REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-20 are pending in the present application, Claims 1, 5, 8, 12, and 19 having been amended. Support for the amendments to Claims 1 and 19 is found, for example in Figs. 1, 4, 11, and 12 and original Claims 5, 8, and 12. Claims 5, 8, and 12 are amended to be consistent with amended Claim 1. Applicants respectfully submit that no new matter is added.

In the outstanding Office Action, Claims 1-4, 7, and 14-16 were rejected under 35 U.S.C. §102(e) as anticipated by Moyer (U.S. Patent No. 6,775,727); Claims 5, 6, 8, 9, 12, and 13 were rejected under 35 U.S.C. §103(a) as unpatentable over Moyer in view of Kendall (U.S. Patent No. 6,836,816); Claims 10, 11, 17, and 18, were rejected under 35 U.S.C. §103(a) as unpatentable over Moyer in view of *Embedded Microprocessor Systems and Design*, by Kenneth Short (hereinafter Short); and Claims 19 and 20 were rejected under 35 U.S.C. §103(a) as unpatentable over Moyer in view of Short, and further in view of Kendall.

Before turning to the rejection of the claims, a brief discussion of the present invention is believed to be in order. In conventional data processors, when an interrupt request occurs during a burst transfer, an interrupt processing is started after the completion of the burst transfer. Therefore, a response to the interrupt request by the data processor is late. Likewise, when a branch instruction to another program is detected during a burst transfer, an instruction to fetch a branch target program is started after the completion of the burst transfer. Therefore, the execution of the branch target program is also late.[1]

In a non-limiting embodiment of the claimed invention, a data processor includes a processor, a first storage device, and a second storage device connected between the

[1] Specification, page 1, lines 17-25.

processor and the first storage device. When a predetermined data required by the processor does not exist in the second storage device, a plurality of data corresponding to one line of the second storage device, including the predetermined data, are read from the first storage device and transferred to a certain line of the second storage device by burst transfer. When an interrupt request occurs during the burst transfer, the burst transfer is suspended and an interrupt processing is started. The data processor also includes an information register that stores information about a request for the predetermined data by the processor while the processor performs the interrupt processing, the information including information about a point at which said burst transfer is suspended. Thus, an interrupt request of high urgency can be started immediately.[2]

With respect to the rejection of Claim 1 as anticipated by Moyer, Applicant respectfully traverses the rejection. Claim 1 recites, *inter alia*, "wherein, when an interrupt request occurs during said burst transfer, said burst transfer is suspended and an interrupt processing is started; and an information register stores information about a request for the predetermined data by said processor while said processor performs the interrupt processing, said information including information about a point at which said burst transfer is suspended." Moyer does not disclose or suggest at least this element of amended Claim 1.

Moyer is directed toward a system and method for controlling bus arbitration during cache memory burst cycles. As shown in Fig. 1 of Moyer, CPU 14 (a bus master) is connected to a global bus 12, along with bus arbiter 34 and alternative bus masters 36, 38, and 40. Bus arbiter 34 functions to control which bus master, within data processing system 10, has a right to use the global bus 12.[3] When bus arbiter 34 receives one or more requests from any of CPU 14 and alternate bus masters 36, 38, and 40, a decision is made as to which

[2] Specification, page 2, lines 4-13.
[3] Moyer, col. 4, lines 65-67.

bus request is serviced first. Such decision may be made on a priority basis, where the bus master with the highest priority is granted access to the global bus.[4]

When an alternative bus master, having a higher priority, requests access to the bus during a burst transfer by another bus master, the master issuing the burst is interrupted, and the master having the higher priority is granted access to the bus[5].

Moyer discloses that reception of a request from one master is stopped when a request from another master is received. On the other hand, in the claimed invention, a request from a same master is temporarily maintained and interrupt processing is carried out first.

"Interrupt" in Moyer is a suspension of a current bus master executing access to the global bus by a request from a different master to access the global bus. A person of ordinary skill in the art would recognize that the claimed "interrupt request" refers to a request, by a device external to the data processor, which signals the data processor that the external device requires service.[6]

Applicants respectfully submit that a request to access a bus by a bus master having a higher priority does not equate to the claimed "interrupt request." Thus, Applicants respectfully submit that Moyer does not disclose or suggest the claimed "wherein, when an interrupt request occurs during said burst transfer, said burst transfer is suspended and an interrupt processing is started; and an information register stores information about a request for the predetermined data by said processor while said processor performs the interrupt processing, said information including information about a point at which said burst transfer is suspended."

Furthermore, a person of ordinary skill in the art would not have been motivated to combine Short with Moyer. Short merely discloses the basics of interrupt processing. Short

[4] Moyer, col. 5, lines 8-11.
[5] Moyer, col. 5, lines 39,46
[6] *See*, Short, page 14, first paragraph.

discloses, on page 502, that the interrupt processing is awaited until the termination of the current instructions. In the claimed invention, on the other hand, a burst transfer is suspended when an interrupt request occurs during a burst transfer.

Moreover, the outstanding Office Action equates the "interrupt" in Moyer to the "interrupt" in Short. However, as the use of "interrupt" is different in Moyer than in Short, such a position is improper.

Furthermore, Kendall does not cure the deficiencies in Moyer or Short. Kendall discloses a configuration to increase the speed of memory access by providing a small cache memory in a main memory.[7] Kendall discloses that a transfer of information from the main memory may be suspended when a request for data that has a higher priority is received. When the interrupting request is finished, the suspended transfer is complete.[8] However, the interrupt of Kendall is different than the "interrupt request" of the claimed invention, at least for the reasons stated above.

In view of the above-noted distinctions, Applicants respectfully submit that Claim 1 (and Claims 2-18 dependent thereon) patentably distinguish over Moyer, Short, and Kendall, taken alone or in proper combination.

Moreover, Applicants respectfully submit that dependent Claim 14 further patentably distinguishes over Moyer, Short, and Kendall. Claim 14 recites, *inter alia*, "a judgment unit comparing a priority of said interrupt request with said predetermined priority...." As recited in Claim 14, the priority is set for the interrupt request. Moyer, on the other hand, discloses that a priority is set for each bus master. Short and Kendall do not cure this deficiency in Moyer.

In addition, Claim 19 recites, *inter alia*, "when a first branch instruction is detected during a first burst transfer in the process of executing a first program, said first burst transfer

[7] Kendall, Abstract.
[8] Kendall, col. 7, lines 23-29.

is suspended and a second program, which is a branch target program, is executed, said data processor further comprising an information register that stores information about a request for the predetermined data by said processor while said processor executes the second program, said information including information about a point at which said burst transfer is suspended." The outstanding Office Action states that Moyer does not disclose these elements recited in Claim 19.[9]

The outstanding Office Action relies on Short to cure this deficiency in Moyer. However, Short does not disclose or suggest suspending a burst transfer when a branch instruction is detected. On the contrary, Short discloses finishing the burst transfer and then executing the branch instruction.[10] For example, Short states "After the 80C188EB completes executing its current instruction, it starts the interrupt processing sequence."[11] Furthermore, page 464 of Short describes how the interrupt request is stored until the processor finishes its task, at which time the processor may start the interrupt processing.

Furthermore, Kendall does not cure the above-noted deficiency in Short. Kendall does not disclose or suggest the claimed "when a first branch instruction is detected during a first burst transfer in the process of executing a first program, said first burst transfer is suspended and a second program, which is a branch target program, is executed, said data processor further comprising an information register that stores information about a request for the predetermined data by said processor while said processor executes the second program, said information including information about a point at which said burst transfer is suspended."

[9] Office Action, page 15, paragraph 39, subsections (r) and (s).
[10] Short, page 502, 463-465, and 475.
[11] Short, page 475.

In view of the above-noted distinctions, Applicant respectfully submits that Claim 19 (and Claim 20 dependent thereon) patentably distinguishes over Moyer, Short, and Kendall, taken alone or in proper combination.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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